What is claimed is:

1. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality M of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

2. The memory system according to claim 1 wherein the memory controller communicates the commands and addresses and the data information using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

3. The memory system according to claim 1 wherein each memory device is a dynamic random access memory device.

4. The memory system according to claim 1 wherein M equals 8.

5. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation; and

a plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a) a plurality M of memory devices;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation.

6. The memory system according to claim 5 wherein the memory controller communicates the commands and addresses using a pipelined packet-protocol which

incorporates a first delay introduced by the buffer register of the plurality of pipelined memory subsystems and a second delay introduced by the data register of the plurality of pipelined memory subsystems.

7. The memory system according to claim 5 wherein each memory device is a dynamic random access memory device.

8. The memory system according to claim 5 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein N equals eight.

9. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a first bidirectional data bus coupled to the memory controller, the memory controller communicating first data information to the bidirectional data bus for a write operation and receiving the first data information from the bidirectional data bus during a read operation;

a second bidirectional data bus coupled to the memory controller, the memory controller communicating second data information to the second bidirectional data bus for a write operation and receiving the second data information from the second bidirectional data bus during a read operation;

a first plurality N of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and

latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the first bidirectional data bus, the data register receiving and latching the first data information from the first bidirectional data bus and driving the first data information to the plurality of memory devices for a write operation, the data register receiving and latching the first data information from the plurality of memory devices and driving the first data information to the first bidirectional data bus for a read operation; and

a second plurality P of pipelined memory subsystems, wherein each memory subsystem includes:

a plurality of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the second bidirectional data bus, the data register receiving and latching the second data information from the second bidirectional data bus and driving the second data information to the plurality of memory devices for a write operation, the data register receiving and latching the second data information from the plurality of memory devices and driving the second data information to the bidirectional data bus for a read operation.

10. The memory system according to claim 9 wherein the memory controller communicates the commands and addresses using a pipelined packet protocol which incorporates a first delay introduced by the buffer register of the first plurality of

pipelined memory subsystems and by the buffer register of the second plurality of pipelined memory subsystems, and a second delay introduced by the data register of the first plurality of pipelined memory subsystems and by the data register of the second plurality of pipelined memory subsystems.

11. The memory system according to claim 9 wherein each memory device of the first plurality of pipelined memory subsystems and each memory device of the second plurality of pipelined memory subsystems is a dynamic random access memory device.

12. The memory system according to claim 9 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and each of the plurality P of pipelined memory subsystems include eight memory devices and further wherein N and P equal 4.

13. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a memory module wherein each pipelined memory subsystem includes:

a plurality M of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus

and driving the commands and addresses to the plurality of memory devices; and

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a socket adapted to receive the memory module and to couple the memory module to the unidirectional command and address bus and to the bidirectional data bus.

14. The memory system according to claim 13 wherein the memory controller communicates the commands and addresses using a pipelined packet-protocol which incorporates a first delay introduced by the buffer register of the memory subsystem and a second delay introduced by the data register of the memory subsystem.

15. The memory system according to claim 13 wherein each memory device is a dynamic random access memory device.

16. The memory system according to claim 13 wherein M equals 8.

17. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a bidirectional data bus coupled to the memory controller, the memory controller communicating data information to the bidirectional data bus for a write operation and receiving the data information from the bidirectional data bus during a read operation;

a plurality R of memory modules wherein at each memory module includes a plurality N of pipelined memory subsystems including:

a plurality of memory devices;

a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices;

a data register connected between the plurality of memory devices and the bidirectional data bus, the data register receiving and latching the data information from the bidirectional data bus and driving the data information to the plurality of memory devices for a write operation, the data register receiving and latching the data information from the plurality of memory devices and driving the data information to the bidirectional data bus for a read operation; and

a plurality of sockets, wherein each socket is adapted to receive one of the R memory modules and to couple the received memory module to the unidirectional command and address bus and to the bidirectional data bus.

18. The memory system according to claim 17 wherein the memory controller communicates the commands and addresses using a pipelined packet protocol which incorporates a first delay introduced by the buffer register of the memory subsystem and a second delay introduced by the data register of the memory subsystem.

19. The memory system according to claim 17 wherein each memory device is a dynamic random access memory device.

20. The memory system according to claim 17 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein the number of sockets equals eight, R equals eight and N equals one.

21. The memory system according to claim 17 wherein each of the plurality N of pipelined memory subsystems includes eight memory devices and wherein the number of sockets equals four, R equals four and N equals two.

22. A memory system comprising:

a memory controller;

a unidirectional command and address bus coupled to the memory controller, the memory controller communicating commands and addresses to the command and address bus;

a first bidirectional data bus coupled to the memory controller, the memory controller communicating first data information to the bidirectional data bus for a write operation and receiving the first data information from the bidirectional data bus during a read operation;

a second bidirectional data bus coupled to the memory controller, the memory controller communicating second data information to the second bidirectional data bus for a write operation and receiving the second data information from the second bidirectional data bus during a read operation;

a first and second memory module, the first and second memory module each having a first memory subsystem and a second memory subsystem; and

a first and second socket, the first socket adapted to receive the first memory module and to couple the first memory module to the unidirectional command and address bus and to the first bidirectional data bus, the second socket adapted to receive the second memory module and to couple the second memory module to the unidirectional command and address bus and to the second bidirectional data bus.

23. The memory system according to claim 22 wherein the first memory subsystem comprises:

a) a plurality of memory devices;

b) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

c) a data register connected between the plurality of memory devices and the first bidirectional data bus, the data register receiving and latching the first data information from the first bidirectional data bus and driving the first data information to the plurality of memory devices for a write operation, the data register receiving and latching the first data information from the plurality of memory devices and driving the first data information to the first bidirectional data bus for a read operation, and further wherein the second memory subsystem includes:

i) a plurality of memory devices;

ii) a buffer register connected between the command and address bus and the plurality of memory devices, the buffer register receiving and latching the commands and addresses from the command and address bus and driving the commands and addresses to the plurality of memory devices; and

iii) a data register connected between the plurality of memory devices and the second bidirectional data bus, the data register receiving and latching the second data information from the second bidirectional data bus and driving the second data information to the plurality of memory devices for a write operation, the data register receiving and latching the second data information from the

plurality of memory devices and driving the second data information to the bidirectional data bus for a read operation.

24. The memory system according to claim 23 wherein the memory controller communicates the commands and addresses using a pipelined packet protocol which incorporates a first delay introduced by the buffer register of the first memory subsystem and by the buffer register of the second memory subsystem and a second delay introduced by the data register of the first memory subsystem and by the data register of the second memory subsystem.

25. The memory system according to claim 23 wherein each memory device of the first memory subsystem and each memory device of the second memory subsystem is a dynamic random access memory device.

26. A method for storing data in a pipelined memory system, comprising the steps of:

communicating commands and addresses to a unidirectional command and address bus;

communicating data information to a bidirectional data bus;

latching the commands and addresses in a plurality of buffer registers;

latching the data in a plurality of data registers;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

driving the latched data to the plurality of memory devices; and

storing the data in the addressable storage of one of the plurality of memory devices.

27. The method of storing information in a pipelined memory system according to claim 26 wherein the step of communicating commands and addresses and the

step of communicating data communicates according to a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

28. The method of storing information in a pipelined memory system according to claim 26 wherein each of the memory devices is a dynamic random access memory device.

29. A method for retrieving data in a pipelined memory system, comprising the steps of:

issuing commands and addresses on a unidirectional command and address bus;

latching the commands and addresses in a plurality of buffer registers;

driving the latched commands and addresses to a plurality of memory devices having addressable storage;

retrieving the data from the addressable storage of one of the plurality of memory devices;

latching the data in a data register; and

receiving the data on a bidirectional data bus.

30. The memory system according to claim 29 wherein each of the memory devices is dynamic random access memory device.

31. The method of storing information in a pipelined memory system according to claim 29 wherein the step of communicating commands and addresses and the step of communicating data communicates according to a packet protocol which incorporates a first delay introduced by the buffer register and a second delay introduced by the data register.

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